LBL HSIO Demux

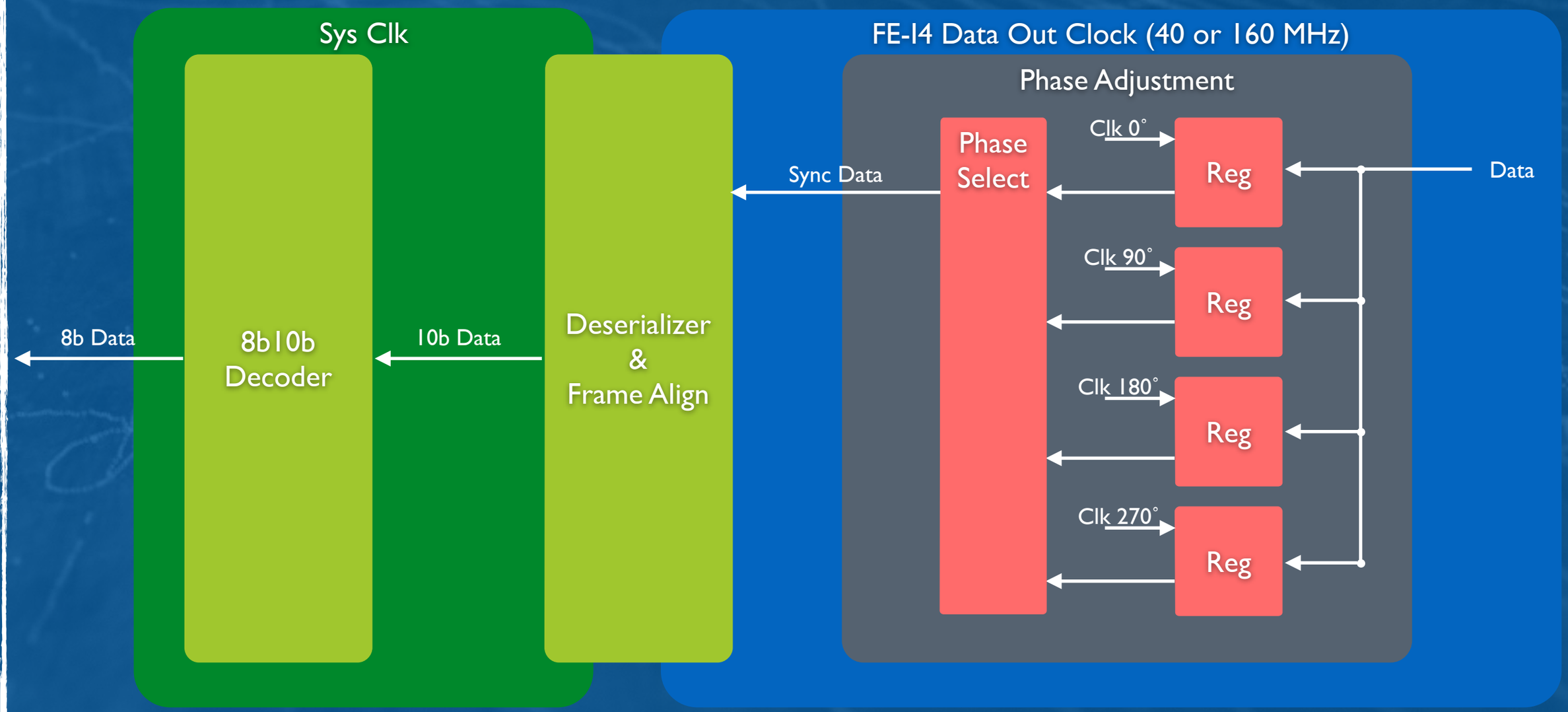
Some notes - 7th of September 2014

Timon Heim

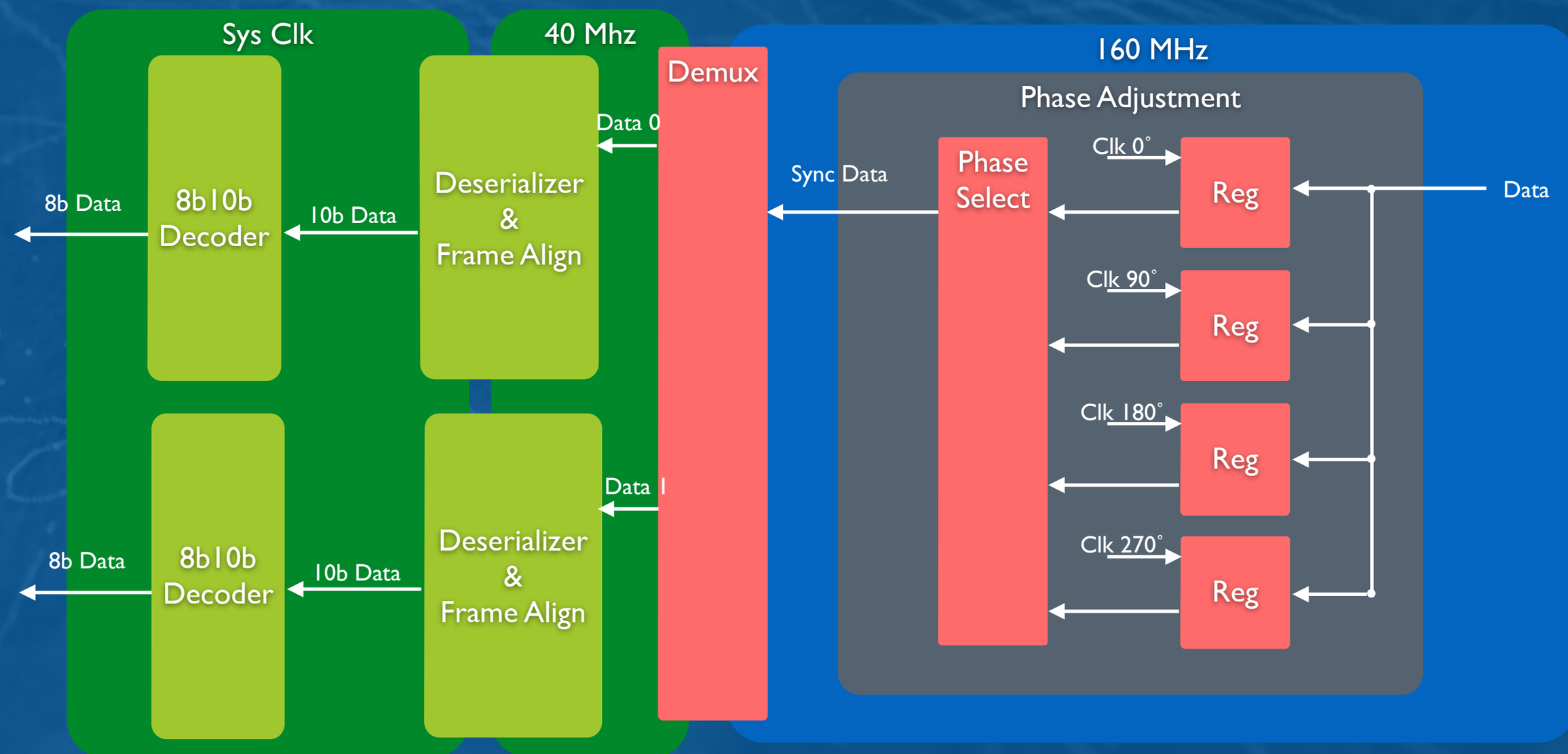
Features

- Hsio firmware specifically for multiplexed Stavelet readout, i.e. two data streams are multiplexed onto one data line
- FE readout with 40 MHz, multiplexed into 80Mbit stream, alternating with 40MHz clock
- Fix 160MHz oversampling in Hsio to find phase
- Demux stream on every second cycle of the 160Mhz clock
- Fix data output of sync block to 40MHz

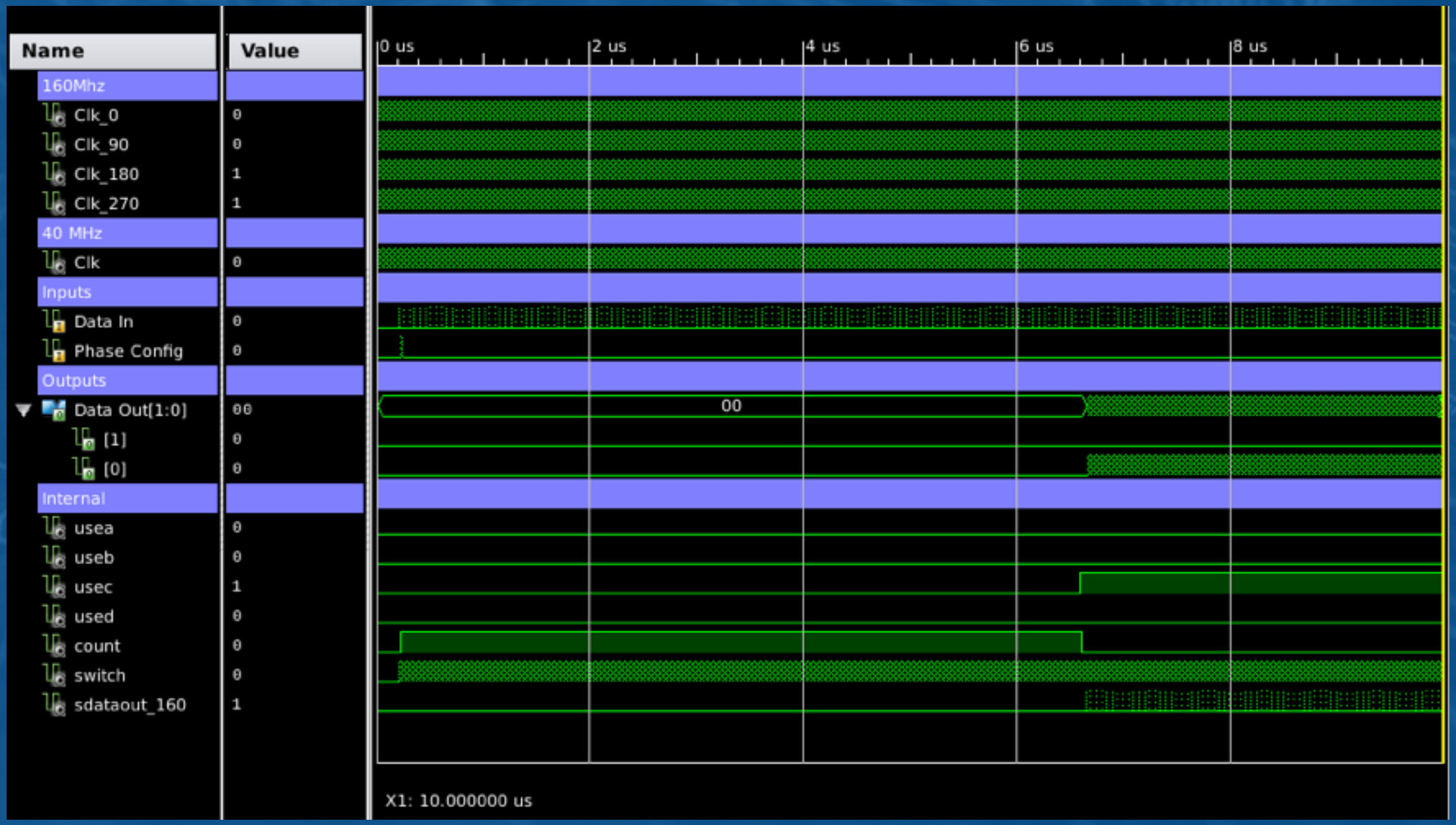
“Standard” Firmware



Demux Firmware

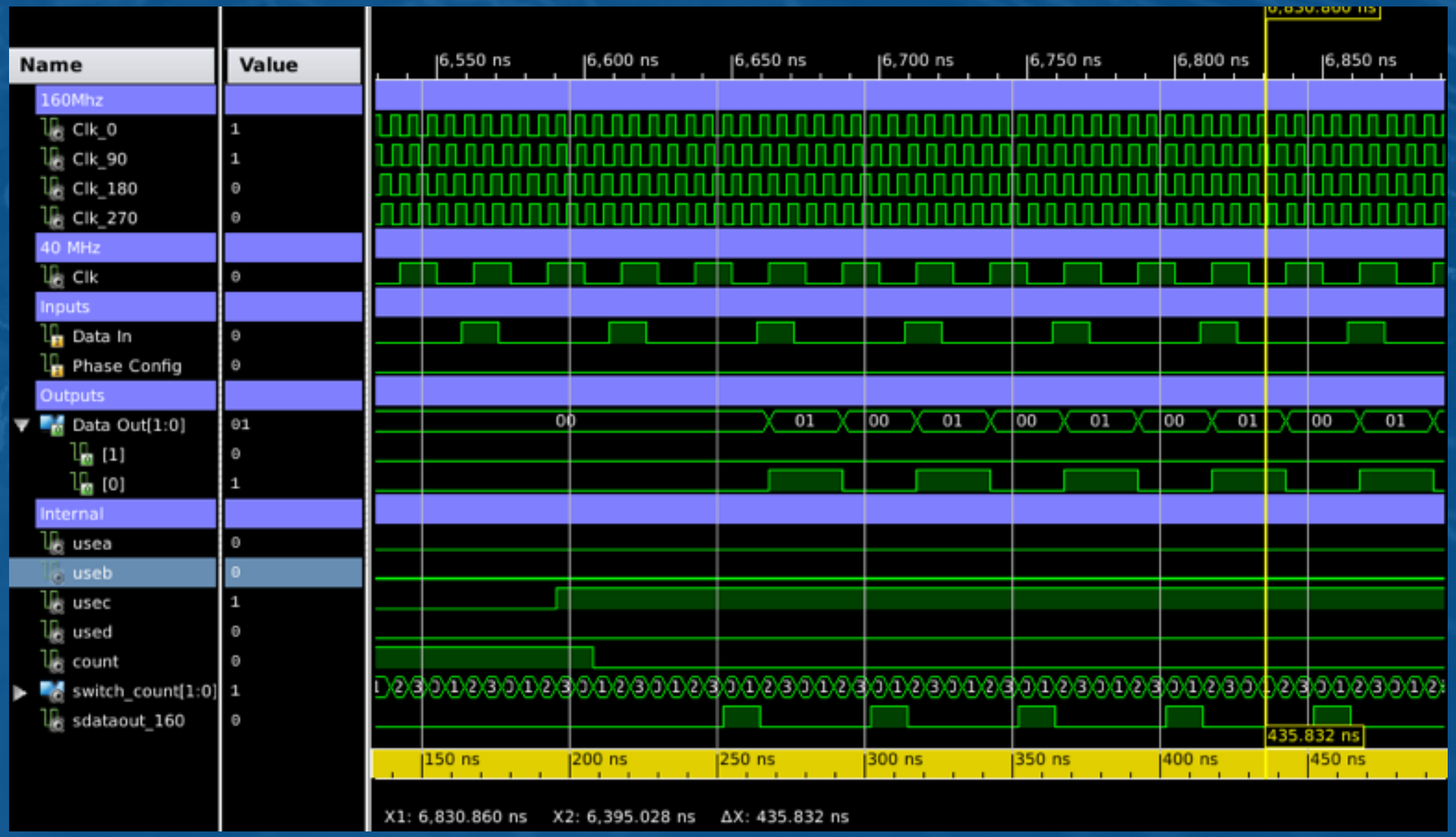


Simulation: Phase Config



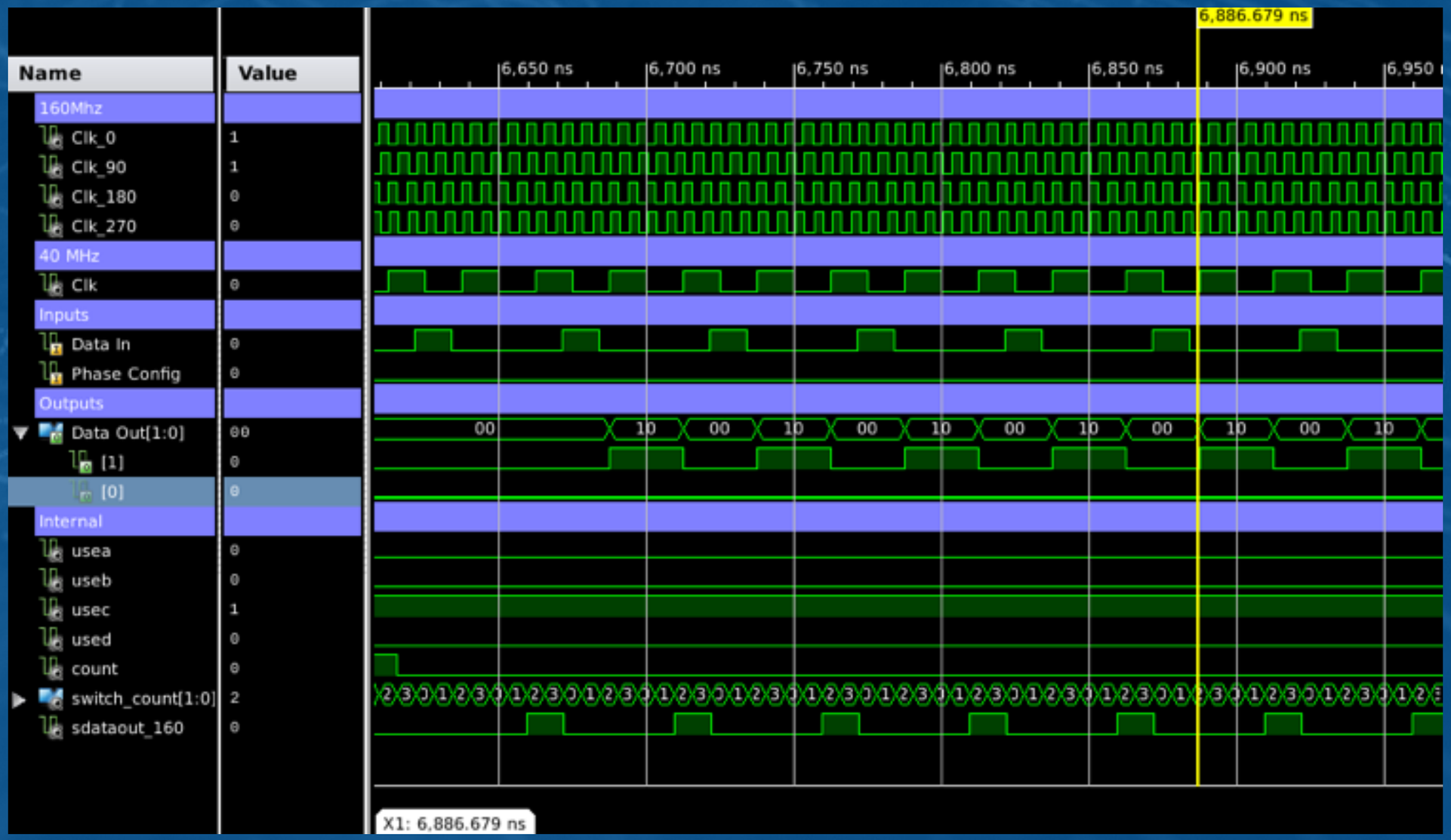
Simulation: Demux

Ch0 pattern = 0x55555555
Ch1 pattern = 0x00000000



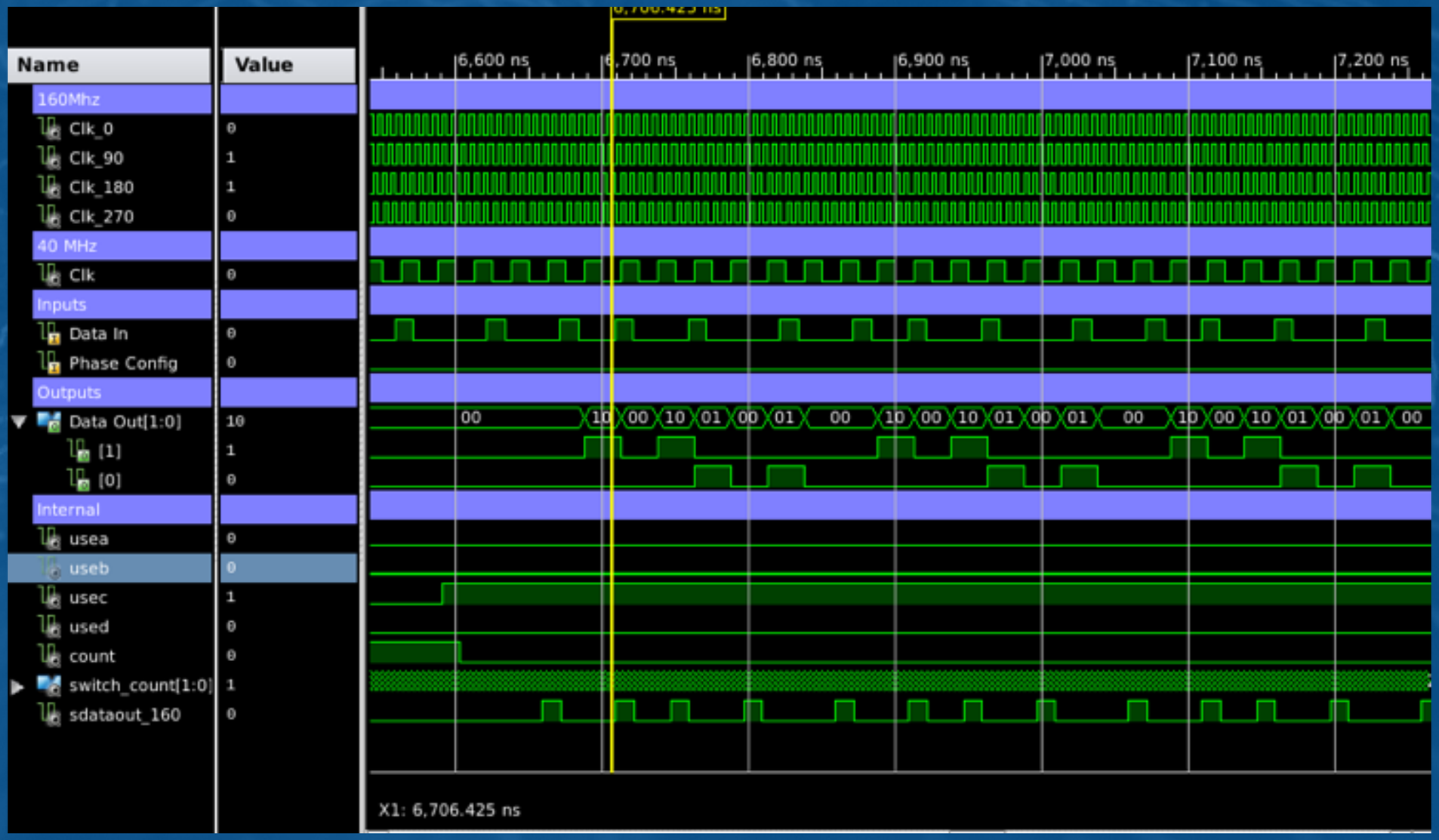
Simulation: Demux

Ch0 pattern = 0x00000000
Ch1 pattern = 0x55555555



Simulation: Demux

Ch0 pattern = 0xAAAAAAAA
Ch1 pattern = 0x55555555

Simulation: Demux

Ch0 pattern = 0x50505050
Ch1 pattern = 0x05050505